PCB Layout Guidelines:

**General Guidelines:**

* Mechanical Board Dimension:
  + Board outline is provided in the PcbDoc file
* Board Thickness: .5mm
* Impedance controlled routing
  + 50 Ohm Single Ended
  + 100 Ohm Differential
* Impedance controlled routing 100 Ohms Differential (See sheet specific notes concerning signals)
* 01005 Capacitors/Resistors can be placed on the bottom side of the board
* PFETs and NFETs (Q?) can be placed on the bottom side of the board
* T1 Can be on the bottom of board

**Sheet Specific Guidelines:**

1. **TOP:** Nothing
2. **Block Diagram:**
   1. Place T1 Connector near the side of the board in order to access the FPGA JTAG.
3. **FPGA:**
   1. Page 3 has an example of an FPGA escape pattern for a 6 layer stackup
4. **FPGA Config:**
   1. Place R33 as close as possible to pin W18
   2. Place all bypass capacitors as close as possible to their respective pins
5. **FPGA Banks:**
   1. Place all bypass capacitors as close as possible to their respective pins
   2. TX\_P/TX\_N are high speed signals and should be routed as 100Ohm differential impedance
   3. TX\_CLK\_P/TX\_CLK\_N are high speed signals and should be routed as 100Ohm differential impedance
   4. RX\_P/RX\_N are high speed differential signals and should be routed as 100Ohm differential impedance
   5. RX\_CLK\_P/RX\_CLK\_N are high speed differential signals and should be routed as 100Ohm differential impedance
6. **FPGA SERDES:** Nothing
7. **FPGA Power:**
   1. All 01005 capacitors should be placed underneath the FPGA
   2. C61 Should be placed close to Banks 0 and 1
   3. C60 Should be placed close to Banks 2 and 3
8. **WIFI Module:**
   1. Place bypass capacitors close to their respective pins
   2. Remove all layers of copper underneath ANT1
   3. 50 ohm trace to ultra mini coax cable
   4. ANT1 is locked
9. **Host Comm:**
   1. TVS pads should be on the traces in a ‘Fly By’ fashion for all the high speed signals and not be layed out in a ‘T’ configuration
   2. R15, R36, R37, R62, R65, R66, R67, R68 pads should be on the traces in a ‘Fly By’ fashion for all the high speed signals and not layed out in a ‘T’ configuration
   3. C\_TX\_P/C\_TX\_N are high speed signals and should be routed as 100Ohm differential impedance
   4. C\_TX\_CLK\_P/C\_TX\_CLK\_N are high speed signals and should be routed as 100Ohm differential impedance
   5. C\_RX\_P/C\_RX\_N are high speed signals and should be routed as 100Ohm differential impedance
   6. C\_RX\_P/C\_RX\_N are high speed signals and should be routed as 100Ohm differential impedance
10. **EPM:**
    1. **P**lace C9 as close as possible to boost converter
    2. Place R13, R14, C10 as possible to U4
    3. The following nets should be as wide as possible:
       1. V28P0
       2. EPMA
       3. EPMB
       4. EPMC
       5. EPMC
       6. EPME
       7. EPMF
       8. EPMG